Claims:

1. A voltage generating circuit comprising:

a first transistor which allows a first current to flow in an emitter thereof;

a second transistor which allows a second current which has a current density larger than a current density of the emitter of the first transistor to flow in an emitter thereof;

a first resistance which is provided between the emitter of the first transistor and the emitter of the second transistor;

a second resistance which is provided between the emitter of the second transistor and a ground potential of the circuit;

a third resistance which is provided between a collector of the first transistor and a power source voltage;

a fourth resistance which is provided between a collector of the second transistor and the power source voltage; and

a differential amplifier circuit having the CMOS constitution which forms an output voltage upon receiving a collector voltage of the first transistor and a collector voltage of the second transistor and, at the same time, supplies the output voltage to bases of the first transistor and the second transistor in common.

2. A voltage generating circuit according to claim 1, wherein the third resistance and the fourth resistance are configured to possess a same resistance value.

3. A voltage generating circuit according to claim 2, wherein an emitter area of the first transistor is set larger than an emitter area of the second transistor.

4. A voltage generating circuit according to claim 3, wherein the first transistor and the second transistor are constituted by making use of a semiconductor region formed in a process of a CMOS circuit which constitutes the differential amplifier circuit.

5. A semiconductor integrated circuit device including a reference voltage generating circuit which comprises:

a first transistor which allows a first current to flow in an emitter thereof;

a second transistor which allows a second current which has a current density larger than a current density of the emitter of the first transistor to flow in an emitter thereof;

a first resistance which is provided between the emitter of the first transistor and the emitter of the second transistor;

a second resistance which is provided between the emitter of the second transistor and a ground potential of the circuit which is supplied from an external terminal;

a third resistance which is provided between a collector of the first transistor and a power source voltage which is supplied from an external terminal;

a fourth resistance which is provided between a collector

of the second transistor and the power source voltage; and

a differential amplifier circuit having the CMOS constitution which forms an output voltage upon receiving a collector voltage of the first transistor and a collector voltage of the second transistor and, at the same time, supplies the output voltage to bases of the first transistor and the second transistor in common.

6. A semiconductor integrated circuit device according to claim 5, wherein the semiconductor integrated circuit device includes a CMOS circuit which is constituted of a second conductive-type well region and a first conductive-type well region which are formed on a first conductive-type semiconductor substrate, a first conductive-type MOSFET which is formed on the second conductive-type well region, and a second conductive-type MOSFET which is formed on the first conductive-type well region, and

the first transistor and the second transistor which constitute the reference voltage generating circuit are formed of a bipolar transistor having the lateral structure which uses diffusion layers which are formed in a step for forming source and drain diffusion layers of the second conductive-type MOSFET which constitutes the CMOS circuit as the collector and the emitter and is operated using the first conductive-type well region on which the diffusion layers which constitute the collector and the emitter are formed as a base.

7. A semiconductor integrated circuit device according to claim 5, wherein the semiconductor integrated circuit device includes the CMOS circuit which is constituted of the second conductive-type well region and the first conductive-type well region which are formed on the first conductive-type semiconductor substrate, the first conductive-type MOSFET which is formed on the second conductive-type well region, the second conductive-type MOSFET which is formed on the first conductive-type well region, and the second conductive-type well region having a depth for electrically separating the first conductive-type well region on which the second conductive-type MOSFET is formed from the first conductive-type semiconductor substrate, and

the first transistor and the second transistor are formed of a bipolar transistor having the vertical structure which uses a second conductive diffusion layer which is formed in a step for forming source and drain diffusion layers of the first conductive-type MOSFET which constitutes the CMOS circuit as the emitter, uses the first conductive-type well region on which the second conductive-type diffusion layer which constitutes the emitter is formed as a base, and uses the second conductive-type well region having a depth which is provided for electrically separating the first conductive-type well region which constitutes the base from the first conductive semiconductor substrate as a collector.

8. A semiconductor integrated circuit device according to claim 5, wherein

the semiconductor integrated circuit device includes a CMOS circuit which is constituted of a second conductive-type well region and a first conductive-type well region which are formed on a second conductive-type semiconductor substrate, a first conductive-type MOSFET which is formed on the second conductive-type well region, and a second conductive-type MOSFET which is formed on the first conductive-type well region, and

the first transistor and the second transistor which constitute the reference voltage generating circuit are formed of a bipolar transistor having the lateral structure which uses diffusion layers which are formed in a step for forming source and drain diffusion layers of the second conductive-type MOSFET which constitutes the CMOS circuit as the collector and the emitter and is operated using the first conductive-type well region on which the diffusion layers which constitute the collector and the emitter are formed as a base.

9. A semiconductor integrated circuit device according to any one of claims 6 to 8, wherein the first conductive-type is a p-type and the second conducive-type is an n-type, and

a power source voltage which is supplied from the external terminal is a positive power source voltage.

10. A semiconductor integrated circuit device according

to claim 9, wherein the second transistor is constituted of one transistor and the first transistor is constituted by connecting a plurality of unit transistors corresponding to the second transistor in parallel.

11. A semiconductor integrated circuit device according to claim 10, wherein the first transistor is configured such that the plurality of unit transistors are formed on the well regions having the same depth, and one of the plurality of unit transistors which are formed to have the same constitution as the first transistor is used as the second transistor.

12. A semiconductor integrated circuit device according to claim 11, wherein

the semiconductor integrated circuit device further includes:

a power source circuit which generates an internal voltage different from a power source voltage which is supplied from the external terminal upon receiving a reference voltage formed by the reference voltage generating circuit;

an internal circuit which is operated by the power source circuit;

an input circuit which is operated upon receiving a power source voltage supplied from the external terminal, performs a level conversion upon receiving an input signal supplied from an external terminal and transmits the signal to the internal circuit; and

an output circuit which is operated upon receiving a power source voltage supplied from the external terminal, performs a level conversion upon receiving a signal generated by the internal circuit, and forms an output signal to be outputted from the external terminal, wherein

the differential amplifier circuit is constituted of a P-channel MOSFET and an N-channel MOSFET which are formed in the same process as MOSFETs which constitute the input circuit and the output circuit which are operated upon receiving a power source voltage supplied from the external terminal.

13. A semiconductor integrated circuit device according to claim 11, wherein

the internal voltage is formed by reducing the power source voltage supplied from the external terminal, and

the internal circuit is formed with a minimum forming size of a CMOS processing.

14. A semiconductor integrated circuit device according to claim 11, wherein

the power source circuit includes a booster circuit and a negative voltage generating circuit which are operated at a constant voltage formed by using the reference voltage, and

a voltage which is formed by the booster circuit and the negative voltage generating circuit is outputted as a gate drive voltage for driving liquid crystal, a source drive voltage corresponding to image data, and a liquid crystal

common electrode drive voltage.